REMARKS

Claims 1-31 are pending and were rejected.

The applicants appreciate the indications that the objection to the Abstract and the Section 101 rejection are withdrawn.

Claims 1 and 12 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner indicated that "the statement: 'preventing, in response to the checking, redundant storage of the new value of the quantity in the computer structure' was not identified in the original disclosure."[1]

The applicants respectfully submit that claims 1 and 12 are properly supported by the written description in the original application. Although the exact language quoted by the Examiner does not appear in the original application, the specification does reasonably convey to one skilled in the art that the inventors had possession of the claimed invention. The primary thrust of the entire application is the prevention of redundant storage in response to checking whether a new value matches a previously stored value. In particular, the Summary of the Invention section on pages 4-5 explains that the invention "provides an improvement by tackling the problem of the redundancy of information due to the storage of the same membership function for different variables or for the same variable ..." (p. 4, lines 9-13) and "makes it possible to optimize the storage space used, **eliminating redundancy**..." (p. 5, lines 1-3). Also, the application explains that block 5 of Figure 1 "is configured in such a way as to implement the algorithm ... which recognizes identical membership functions, **stores only one of these for each type**, and recompiling the fuzzy inferences in such a way that the pointers to identical membership functions converge on the single membership function stored in a corresponding store indicated by 6" (p. 5, line 25 – p. 6, line 2). Similar statements are made at page 7, lines 25-29 and page 8, lines 15-19.

In view of the entire specification, including the particular lines referenced above, one skilled in the art certainly would understand that the inventors had possession of the

[1] The applicants assume that by using the word "identified" the Examiner did not intend to imply that the quoted language must be identically used in the specification. Such identical usage is not required by Section 112, as noted by numerous Federal Circuit cases. *E.g., All Dental Prodx, LLC v. Advantage Dental Products, Inc.*, 309 F.3d 774, 779, 64 USPQ2d 1945 (Fed. Cir. 2002).

invention, at the time the application was filed, including "preventing, in response to the checking, redundant storage of the new value of the quantity in the computer structure." Accordingly, claims 1 and 12 are properly supported by a written description of the invention.

Claims 1-31 were rejected under 35 U.S.C. § 102(a) as being anticipated by an article entitled "Dynamic-Link Rule Base in Fuzzy Inference System" by Lin.

In the Amendment filed November 24, 2003, the applicants showed that Lin does not anticipate claims 1-22 for two reasons. First, the applicants submitted a Rule 131 Declaration to show that Lin was not published before the claimed invention was made. Second, the applicants explained why Lin does not disclose the claimed invention. The applicants continue to assert both reasons, but will address second reason first because it logically follows the above discussion of the Section 112 rejection.

As pointed out in the November 24 Amendment, Lin does not disclose the invention of claims 1-22 because Lin does not check in a computer store for already-stored values that match a new value of a membership function or operand and does not prevent redundant storage of such a new value. In fact, the entire point of Lin is to create a dynamic link rule base that is a redundant sub-set of an original rule base. Lin simply compares an input value with a premise part of each of numerous fuzzy rules stored in the original rule base and copies those fuzzy rules having a non-zero firing strength, based on the comparison, into the dynamic link rule base. Nothing in Lin suggests a method of preventing redundancy in the original rule base by itself; in the dynamic link rule base by itself; or in the dynamic link rule base compared to the original rule base.

The applicant's respectfully submit that the Examiner's response to that argument is insufficient to support the Section 102 rejection. The Examiner does not indicate how or where Lin prevents redundant storage, but instead simply states that "the issue of redundant storage was appropriately addressed at para 6 as new matter." Assuming that the Examiner intended to refer to the written description rejection in paragraph 8 of the Office Action, the Examiner's statement is insufficient for at least two reasons. First, as discussed above, the language of claims 1 and 12 are properly supported by the written description in the application as filed. Second, to support a Section 102 rejection, Lin must disclose every feature of the

claims, including the prevention of redundancy feature, regardless of whether the feature is new matter or supported by a written description. Section 706.03 (o) of the MPEP states that "As to any other appropriate prior art or 35 U.S.C. § 112 rejection, **the new matter must be considered as part of the claimed subject matter and cannot be ignored**" (see Examiner note 3 immediately before Section 706.03 (s)). Given the applicants' showing that Lin does not disclose the redundancy prevention feature of claims 1-22 and that the Examiner has not pointed to anything in Lin as disclosing that feature, Lin does not anticipate claims 1-22.

Lin also does not disclose the invention recited in claims 23-28. In particular, Lin does not disclose fuzzy inference encoding means that compares an encoded input membership function to a stored membership function, stores a pointer to a matching stored membership function, stores the encoded input membership function if a match is not found, or store a pointer to the stored encoded input membership function. Instead, Lin simply compares an input value to stored fuzzy rules without comparing fuzzy rules or membership functions to each other. Without comparing membership functions, Lin cannot possibly store a pointer and/or store an encoded input membership function based on such a comparison. Accordingly, Lin does not anticipate claims 23-28 regardless of the published date of Lin.

The applicants respectfully disagree with the Examiner's response, which relies on the following statement on page V-247 of Lin: "The purpose of the rule selector is to pick out the fired rules and reject the non-fired rules." First, as shown in Fig. 2 of Lin, the rule selector compares a crisp input value (i.e., an unencoded value) to the fuzzy rules of the original rule base rather than comparing an **encoded** input membership function to a stored encoded membership function. Second, the input value is simply a value prior to fuzzification and is not a membership function. As shown on page V-248 of Lin, the crisp input value x_1 is converted to five membership functions $A_1^{(1)}(x_1)$ - $A_1^{(5)}(x_1)$, but those membership functions are never sent to the rule selector for comparison to any stored membership functions.

The applicants also disagree with the implication in the Examiner's response that Lin discloses the pointer storing steps of claim 23 because "to one of ordinary skill in the art, pointers are generic." If by "generic" the Examiner is asserting that pointers are inherent to Lin's system, then the applicants disagree. Nothing in Lin's system inherently requires "storing

with the encoded fuzzy inference a pointer to the matching stored encoded membership function," if a stored encoded membership function is found to match the encoded input membership function, or "storing the encoded input membership function in the membership function storage device and storing with the encoded fuzzy inference a pointer to the stored encoded input membership function," if none of the stored encoded membership functions is found to match the encoded input membership function. As pointed out in pages 1-4 of the present application, the prior art fuzzy systems do not store pointers to matching stored encoded membership functions, and thus, the pointer storing steps of claim 23 cannot be inherent in any system. Further, one could create the dynamic link rule base by simply copying the fired rules from the original rule base, and thus, no pointers would be necessary.

Accordingly, Lin does not anticipate claims 23-28.

Although the language of claims 29-31 differs from that of claims 23-28, several distinguishing features of claims 29-31 will be apparent in view of the above discussion.

As mentioned above, Lin also does not anticipate claims 1-31 under section 102(a) because Lin was not published before the claimed invention was made. According to the copy of Lin received from the Examiner, Lin was published October 12-15, 1999. The European patent application 00830082.4, from which the present application claims priority, was filed on February 8, 2000. Enclosed with the November 24 Amendment was a Rule 131 Declaration signed by one of the inventors, Francesco Papalardo, showing that the claimed invention was conceived prior to October 12-15, 1999 and was diligently reduced to practice with the filing of the priority European patent application 00830082.4. In support of the Declaration were a Patent Proposal (Appendix A) dated September 28, 1999 (with English translation), which describes the claimed invention in detail, and three documents (Appendixes B-D) with English translation showing diligent steps to reduce the invention to practice. Accordingly, Lin was not published before the claimed invention was made, and thus, claims 1-31 are not anticipated by Lin under section 102(a).

The Examiner responded to the Rule 131 Declaration with several comments/questions that called into question the effectiveness of the Declaration. The applicants submit that the items mentioned by the Examiner should not render the Declaration

insufficient to establish that the invention was made before the publication of Lin. Most of the items are due to the fact that the relevant documents are in Italian. The items are address as follows using the Examiner's organization:

A. Attached is a photocopy of Appendix A which includes the inventors' signatures on the second page. The second page of Appendix A is in English, so the applicants have not changed the translation of the Italian portions of Appendix A.

B. The original patent proposal from the inventors mistakenly identified the third inventor as Marcello Palano. The spelling of the third inventor's name is correctly shown as Carmelo Palano in the USPTO records.

C. The translation of the Italian portions of Appendix A did not include Figures because the Figures were included in Appendix A and it did not seem necessary to include another copy. Attached are Figures 1 and 2 of Appendix with the Italian captions replaced with English captions for the Examiner's convenience.

D. It seems clear from Appendix A that the reference to prior art concerning fuzzy theory is omitted by the inventor solely because its inclusion would be unnecessary duplicative and not essential to the understanding of the invention. It is unclear how that raises an issue of double patents or otherwise detracts from the persuasiveness of the Declaration.

E. The translated Appendix A is an accurate English translation of the Italian portions of Appendix A. As discussed above, Figure 1 was provided with the original Appendix A in Italian and the translations of the captions of Figure 1 were provided in the translation. Pages 4-8 of the translation discuss the various circuit components. The applicants do not understand how translated Appendix A raises any serious questions. The Figures 1-2 of Appendix A are substantially identical to Figures 1-2 of the present application except that the Figures 1-2 of Appendix A do not include reference numbers.

F. The original document included in Appendix B mistakenly identified the third inventor as Marcello Palano. The spelling was corrected to shown Carmelo Palano as third inventor.

G. Appendix B refers only to the possibility of disclosure by January 31, 2000, which did not happen.

H. See G.

I. The draft application mentioned in Appendix C was not provided because the draft application is not available at this time. In view of the letter of Appendix C and the email letter from the inventor in Appendix D, it seems clear that the draft application was enclosed with the letter of Appendix D.

J. The Examiner notes that the Declaration has only the signature of one inventor out of three. This should not detract from the effectiveness of the Declaration for at least two reasons. First, the applicants are unaware of any rule requiring all of the inventors to sign such a Declaration. Second, the Declaration and attachments included numerous pages in both Italian and English, which would necessitate a large amount of time from the other inventors and take the other inventors away from their primary job of inventing.

K. Additional internal documents have not become available.

L. No inventor logs are believed to exist.

In view of the above explanations, the applicants submit that the Declaration and Appendices do show that the invention was conceived prior to the publication of Lin and was diligent reduced to practice with the filing of the priority European patent application 00830082.4. Accordingly, the applicants respectfully request the Examiner to reconsider his response to the Declaration.

In paragraph 4 on page 2, the Examiner encourages the applicants to respond specifically to all points made in the office action and states that this was not done in response to the first Office Action. The applicants' attorney always tries to respond to all objections and rejections included in office action and believes that the Amendment filed on November 24, 2003 did respond specifically to all of the objections and rejections. In particular, the first Office Action included an objection to the Abstract and rejections under sections 101 and 102. As indicated above, the November 24 Amendment overcame the objection and the Section 101 rejection. Also, the November 24 Amendment included amendments to some of the claims and detailed remarks showing why the cited reference did not anticipate the pending claims. As such, the applicants do not understand which points were not responded to.

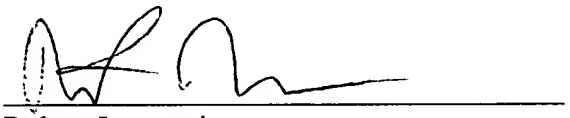
The applicants have again attempted to respond to all of the Examiner's points. If the Examiner continues to feel that this Response is not fully responsive, the Examiner is encouraged to contact the applicants' attorney for a telephone interview, so that the applicants can be more responsive.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Robert Iannucci
Registration No. 33,514

RXI:lmt

Enclosure:
Postcard
Appendix A
(2) Sheets of Drawings – Translation of Fig. 1-2 of Appendix A

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500041_1.DOC

APPENDIX A

PATENT PROPOSAL 99-CT-302

5-10-99

*** CONFIDENTIAL ***

Codice attributo: 5.10.99

Descriptive Title of Invention:

METODO E STRUTTURA PER L'OTTIMIZZAZIONE DELLA CODIFICA E COMPUTAZIONE DELL'INFERENZA FUZZY

Inventor(s):

1) First Name: Francesco Family Name: Pappalardo
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1. *Date of conception of invention:* luglio 1999

2. *Date of reduction to practice of invention:* --------

   Describe how, where and to what extent the invention was reduced to practice.

3. *Was any of the work performed under a contract with third party?* NO

   What party ? ---------- ***Attach copy of contract***

4. *Has there been:*

   1) any disclosure of the invention outside of the company ? NO *when ?* ----------

   Give details

   2) any sampling or sale of products embodying the invention ? NO *when ?* ----------

   Give details

5. *When do you expect any such disclosure or sampling or sale ?* Q1 anno 2000

   Give details

6. *Is the invention related to any other invention / Patent Application ?* NO

   which one(s) ? ----------

7. ***Prior Art:*** *Description of the technological background and of the state of the art, including references to products, patents, articles, etc. known to you (both from your company and others), useful for understanding the invention and for determining its scope.*

8. ***Description of Invention:*** *Brief explanation of what the invention is, how it differs from Prior Art, and what advantages and disadvantages it has with respect to the Prior Art, and detailed and complete explanation of the invention (both structural and functional) making reference to drawings.*

9. ***Signatures of inventors with Date of signature:***

Francesco Gallarda _____ *Date:* 28/09/99

Mirko Fiandone _____ *Date:* 28/9/99

Carlo Adduci _____ *Date:* 28/9/99

_____ *Date:* _____

Enclosures:

- ☐ *Attached hereto are ( ) Prior Art documents [see item 7 above]*
- ☒ *Attached hereto are (7) pages of Description of the Invention [see item 8 above]*
- ☐ *Attached hereto are ( ) pages of examplifying drawings / sketches*
- ☒ *Attached hereto is a product classification page !!!*

1 - Category of the invention

Indicate one letter in the following list that better fits to the invention

☒	**D** - Device	Silicon structure or part of it and its way of working
☐	**C** - Circuit	Electric circuit, even if some of its parts are represented by blocks, and its working
☐	**S** - System	Everything above circuit level, like architectures and methodologies; usually described with a block diagram
☐	**F** - Frontend	Steps, methodology and manufacturing machines or tools to get to the product before its testing; typically silicon processes
z	**B** - Backend	Testing, Packaging, Bonding, Assembly and everything after testing

2 - Product Codes: _____

Indicate the real-product codes in which the invention is or will be used - e.g. TDA123, U012, ...

3 - Product Classes

Indicate one or more words that better describe the products the invention applies to

☐	**A/D**	Analog to digital converters
☐	**AGC**	Automatic Gain Control systems
☐	**AMPLIFIER**	Amplifiers architectures and circuits
☐	**ANALOG**	Products for analogic applications; always used in combination with another word (for example CMOS ANALOG)
☐	**AUDIO**	Every device, circuit or system Audio- or Radio- dedicated
☐	**AUTO**	All the products for automotive applications (Ignition, Injection and Instrumentation)
☐	**BATTERY**	Battery chargers and accessories
☐	**BCD**	BCD technology
☐	**B/E**	Everything in backend that is not Packaging or Testing
☐	**BICMOS**	BICMOS technology
☐	**BIPOLAR**	Bipolar technology and devices
☐	**CCD**	CCD devices
☐	**CMOS**	CMOS devices, circuits and technology
☐	**COMPUTER**	Everything applies to Computers and is not included in GRAPHICS, PERIPHERAL and PROCESSORS which are defined below
☐	**D/A**	Digital to analog converters
☐	**DESIGN**	Products and methods to carry out design
☐	**DIODE**	Diode devices
☐	**DISPLAYS**	Circuits, devices and architectures for displays and mónitors
☐	**DRAM**	DRAM memory cells and circuits
☐	**DRIVERS**	Circuits and systems to drive Hard-Disks and to interface with them
☐	**EPROM**	EPROM memory cells and circuits
☐	**EEPROM**	EEPROM memory cells and circuits
☐	**F/E**	Everything in frontend which cannot be classified with other words of this list, such as machine and tools used in silicon processes

- ☐ **FIFO** FIFO memories
- ☐ **FILTER** Analog and digital filters
- ☐ **FLASH** FLASH memory cells and circuits
- ☒ **FUZZY** Fuzzy logic processors, architectures and methods
- ☐ **GRAPHICS** Graphic processors
- ☐ **HCMOS** HCMOS technology and devices
- ☐ **HPD** High Power Devices
- ☐ **IGBT** IGBT devices and technology
- ☐ **ISDN** ISDN protocols and relative circuits
- ☐ **LAMP** Lamp driver devices and circuits (Light Ballast)
- ☐ **LOGIC** All logic circuits (FLIP-FLOPs ...), families (TTL ...) and interfaces
- ☐ **MODEM** Circuits and systems for modems
- ☐ **MOS** MOS devices and technology
- ☐ **MOTORS** Everything deals with electric motors, such as drivers or regulators
- ☐ **MPEG** Everything deals with MPEG
- z **NEURAL** Neural networks and their applications
- ☐ **NVRAM** NVRAM memories
- ☐ **PACKAGING** Packages and their manufacturing methods
- ☐ **PASSIVE** Passive devices (Resistors, Inductors, Capacitors)
- ☐ **PERIPHERAL** Peripheral controllers and interfaces
- ☐ **PIC** Power Integrated Circuits, such as integrated drivers and controllers of an output power stage
- ☐ **PLA** Devices, circuits and systems for Programmable Linear Arrays
- ☐ **POWER BIPOLAR** Power Bipolar transistors and technology
- ☐ **POWER MOS** Power MOS technology and devices
- ☐ **POWER ON RESET** Circuits or devices to initialize a system at switching on
- ☐ **POWER SUPPLY** Circuits and systems for supplying power, such as e.g. generators
- ☐ **PROCESSORS** Used together with Peripheral and Graphics to better specify Computer products classification
- ☐ **PROTECTION** Protection circuits, devices and systems (against overvoltages, ovecurrents, ElectroStatic Discharge ...)
- ☐ **REGULATOR** Voltage regulators, stabilizers, elevators and every circuit that fixes a defined voltage
- ☐ **ROM** ROM memory cells and circuits
- ☐ **SENSORS** Sensing devices and relative circuitry
- ☐ **SHADOW RAM** SHADOW RAM memories
- ☐ **SLIC** Telecom circuits and systems on the Central Office's side
- ☐ **SMART POWER** Smart Power applications
- ☐ **SRAM** SRAM memory cells and circuits
- z **TESTING** methods, circuits and apparatuses for testing
- ☐ **TELEPHONE SET** Telecom circuits and systems on the Subscriber's side
- ☐ **TV** All circuits and devices for TV sets
- ☐ **VIPOWER** Products in VIPOWER technology or modifications to process steps

PROPOSTA DI BREVETTO

METODO E STRUTTURA PER L'OTTIMIZZAZIONE DELLA CODIFICA E COMPUTAZIONE DELL'INFERENZA FUZZY

Autori: Pappalardo Francesco, Giacalone Biagio, Palano Marcello

Premessa

Si omette tutta l'arte nota sulla teoria fuzzy poiche' ripetuta piu' volte nei nostri precedenti brevetti e focalizziamo solo i concetti fuzzy necessari per la descrizione della presente proposta di brevetto.

Ricordando che nel processamento fuzzy abbiamo:
- Variabile di ingresso;
- Fuzzy set della variabile di ingresso;
- Membership Function contenute nei fuzzy set;
- Operatori fuzzy And ed OR;
- Conseguente.

L'inferenza fuzzy o regola fuzzy utilizzata nella computazione fuzzy e', secondo la teoria Fuzzy, del tipo:

If antecedente THEN conseguente

dove in particolare la parte antecedente puo' essere essere esplosa in:

ing0 is/not_is MF0 and/or ing1 is/not_is MF1 .....
..... and/or ing_n is/not_is MF_n .

Quindi la generica regola fuzzy, come quella sopra indicata, consta di un antecedente composto da condizioni atomiche, come " **ing0 is/not_is MF0**" che per brevita' indichiamo come "**V is/not_is M** ", legata da connettivi logici, come AND, OR.

La condizione atomica esprime il grado di appartenenza di un elemento dell'universo del discorso ad un particolare sottoinsieme fuzzy di tale universo. L'elemento in esame e' denotato dalla variabile di ingresso V ed il sottoinsieme fuzzy e' caratterizzato dalla funzione di appartenenza M.

Inoltre, la regola fuzzy viene codificata e memorizzata all'interno della struttura che dovra' computarla.

Tutti i metodi di memorizzazione dell'inferenza fuzzy e della relativa base della conoscenza, associano (analogamente a quanto fatto nella teoria fuzzy) ad ogni ingresso il suo set di membership, ovvero la relativa base della conoscenza che contiene tutte le membership utilizzate dalla variabile di ingresso.

Per il calcolo dell'inferenza fuzzy tramite una struttura atta a computarla, l'U.d.D. delle M.F. di tutte le variabili di ingresso viene traslata in un U.d.D. base, in modo tale che sia possibile

la computazione dell'inferenza fuzzy. Considerando una struttura di calcolo digitale, l'U.d.D. base per tutte le M.F. sara' mappato su un insieme discreto che va' da 0 a (2^n)-1 dove n e' il numero di bit fissato come dimensione per tutte le variabili d'ingresso.

Problemi riscontrati che si vogliono ottimizzare

1) Le diverse variabili di ingresso hanno quasi sempre i campi dell'universo del discorso completamente diversi tra loro, quindi le membership sono formalmente diverse, inoltre anche se hanno lo stesso U.d.D. non e' facile riconoscere due M.F. uguali se sono descritte in modo grafico.

Inoltre, spesso nell'U.d.D. base, per le diverse variabili di ingresso, vi sono membership uguali tra loro e quindi nella memorizzazione all'interno della struttura che li deve computare vengono ripetute per ogni variabile di ingresso a cui sono associate.

Quanto detto fino ad ora, ovvero il problema della ridondanza dell'informazione dovuta alla memorizzazione della stessa M.F. per diverse variabili o per la stessa variabile, non e' stato fino ad ora ottimizzato.

2) Le diverse condizioni atomiche " **ing0 is/not_is MF0**", opportunamente calcolate, determinano i valori chiamati **alfa** (che risultano essere gli operandi della parte antecedente). Tali condizioni atomiche si calcolano come il punto di intersezione tra la variabile di ingresso **ing0** e la membership function **MF0**; tale calcolo risulta essere una operazione onerosa in termini di tempo e nel calcolo totale dell'inferenza occupa buona parte del tempo di calcolo.

Idea alla base della proposta brevetto

Come detto precedentemente, le diverse variabili di ingresso hanno quasi sempre i campi dell'universo del discorso completamente diversi tra loro, e per ognuno nel proprio campo di esistenza vengono descritte le membership adatte per il tipo di operazione fuzzy che si deve effettuare. Tali membership pero', per essere utilizzate dall'unita' di calcolo hardware che computa le inferenze, devono essere rimappate dall'universo del discorso della variabile in un intervallo discretizzato adatto all'unita' di calcolo. Questa operazione deve essere fatta per tutti gli universi del discorso delle variabili di ingresso utilizzati nelle inferenze da computare.

Si e' osservato che dopo il rimappaggio nell'universo del discorso, molte MF risultano uguali, sia tra quelle della stessa varibile di ingresso che molto spesso tra variabili di ingresso diverse.

Inoltre si e' osservato che molto spesso il valore della variabile V (che e' un ingresso al nostro sistema) usata per il calcolo dell'alfa, cambia con una frequenza molto bassa quindi ciclicamente si calcola piu' volte lo stesso valore di alfa.

La proposta di brevetto di seguito indicata ci permette:

1) di ottimizzare lo spazio di memoria utilizzato eliminendo le ridondanze;

2) di ottimizzare il tempo di esecuzione della inferenza conservando in una memoria di supporto i valori alfa calcolati.

Il circuito considerato e' mostrato nella figura 1.

Dal circuito si noti il blocco "Gestore Caricamento Inferenze Fuzzy", in tale blocco si ha il circuito che implementa l'agoritmo sotto descritto che in fase di caricamento delle MF e delle Inferenze Fuzzy, riconosce le MF uguali, ne memorizza solo una e ricompila le inferenze fuzzy cosi che' i puntamenti alle MF uguali convergano sull'unica MF (di quel tipo) memorizzata.

Inoltre si noti il blocco "Unita' di controllo processamento regole fuzzy" che nel caso di calcolo del valore alfa implementa l'algoritmo di ricerca dell'eventuale alfa gia' calcolato e quindi memorizzato nella "Memoria di Supporto" e nel caso in cui non lo trova, esso lo calcola ed oltre a utilizzarlo per l'inferenza, lo memorizza nella memoria di supporto insieme alla relativa MF ed al valore di ingresso che lo hanno generato.

Algoritmo di caricamento delle MF e delle inferenze Fuzzy

Come gia' detto, per il calcolo dell'inferenza fuzzy tramite una struttura atta a computarla, l'inferenza fuzzy (in seguito chiamata IF) viene codificata per poterla memorizzare all'interno della struttura di calcolo, in questa codifica si ha anche che l'U.d.D. delle M.F. di tutte le variabili di ingresso viene traslata in un U.d.D. base, in modo tale che sia possibile la computazione dell'inferenza fuzzy.

Considerando una struttura di calcolo digitale, l'U.d.D. base per tutte le M.F. sara' mappato su un insieme discreto che va da 0 a (2^n)-1 dove n e' il numero di bit fissato come dimensione per tutte le variabili d'ingresso.

Dopo queste operazioni, si ha quindi la codifica della IF che chiamo IF' e la codifica della M.F. che chiamo M'.

Il metodo di memorizzazione non ha assolutamente importanza per la nostra proposta di brevetto poiche' noi partiamo dalle I.F. e dalle M.F. codificate con un qualsiasi metodo.

Una caratteristica comune a tutti i metodi di codifica e' che la IF' deve contenere le descrizioni delle M' necessarie per il calcolo degli alfa.

La nostra proposta di brevetto e' il circuito racchiuso nel blocco "Gestore caricamento inferenze fuzzy", che gestisce la memorizzazione delle IF' e delle M' all'interno della struttura di calcolo.

In particolare il nostro circuito riconosce se una IF' sta' puntando ad una M' uguale ad un'altra gia' memorizzata e quindi rindirizza il puntamento a quest'ultima risparmiando area di memoria.

Considerando che una realizzazione possibile del nostro circuito e' l'implementazione di una macchina a stati, possiamo descrivere in termini di algoritmo una delle tante implementazioni possibili tramite macchina a stati del circuito hardware oggetto della nostra proposta di brevetto, in particolare la macchina a stati dovra' eseguire le seguenti operazione:

A) RICEVE DALL'ESTERNO IN MODO SERIALE LA IF' DA MEMORIZZARE
B) MEMORIZZA LA IF' FINO ALLA PRIMA CODIFICA M'
C) VERIFICA CHE LA CODIFICA M' E' PRESENTE O MENO IN MEMORIA E QUINDI:
C1) SE NON E' PRESENTE IN MEMORIA, LA MEMORIZZA E SCRIVE NELLA IF' IL SUO PUNTAMENTO

C2) SE E' PRESENTE (PERCHE' E' UGUALE AD UN'ALTRA GIA' MEMORIZZATA), PRELEVA IL PUNTATORE ALLA M' GIA' MEMORIZZATA E LA SCRIVE IN IF' (IN QUESTO MODO ACCORPO LE DUE MF UGUALI)

D) RITORNA AL PUNTO A) FINO A QUANDO NON FINISCONO LE IF' DA MEMORIZZARE.

Algoritmo di ricerca, di calcolo e di memorizzazione del valore alfa

Come gia' detto, molto spesso il valore della variabile V (che e' un ingresso al nostro sistema) usata per il calcolo dell'alfa, cambia con una frequenza molto bassa quindi ciclicamente si calcola piu' volte lo stesso valore di alfa.

La nostra proposta di brevetto serve a risparmiare tempo nel calcolo dell'inferenza fuzzy e quindi risparmiare risorse per dedicarle agli altri processamenti svolti dalla nostra struttura di calcolo.

La nostra proposta di brevetto, procede a determinare un valore di alfa tramite ricerca del valore nella memoria di supporto e, se non lo trovasse, calcola il valore alfa e oltre che renderlo disponibile al calcolo dell'inferenza totale, lo memorizza nella memoria di supporto.

Tale memoria di supporto e' utilizzata come una memoria stack con caricamento dall'alto e svuotamento dal basso. In particolare in tale memoria gli alfa, man mano che vengono calcolati, vengono memorizzati dall'alto verso il basso, mentre i valori che vengono trovati all'interno della memoria, sono fatti risalire fino al punto piu' alto (punto di ingresso dei nuovi calcolati). Man mano che la memoria viene riempita, si perdono i valori memorizzati nel punto piu' basso.

Considerando sempre che una possibile realizzazione del circuito hardware da noi descritto puo' essere sempre una macchina a stati, in termini di algoritmo tale circuito hardware esegue le seguenti operazione:

A) RICEVE I PARAMETRI PER IL CALCOLO DELL'ALFA, OVVERO LA VARIABILE DI INGRESSO V E IL PUNTATORE ALLA M' CHE CHIAMO PM

B) PROCEDE AL CALCOLO DEL VALORE ALFA E PARALLELAMENTE PROCEDE ALLA RICERCA DELL'EVENTUALE VALORE GIA' CALCOLATO TRAMITE I VALORI V E PM.

IN PARTICOLARE NELLA MEMORIA DI SUPPORTO PER I VALORI DI ALFA CALCOLATO, VENGONO MEMORIZZATI { [V, PM], [ALFA] } (si veda fig. 2). CON ALFA CHE E' IL VALORE CALCOLATO CON QUEL VALORE DI V E CON LA M' PUNTATA DA PM, INOLTRE E' UNA MEMORIA DI TIPO A PILA CON CARICAMENTO DALL'ALTO.

QUINDI LA RICERCA SI FA' CONTROLLANDO CHE I VALORI V E PM RICEVUTI IN A) SIAMO UGUALI A QUELLI MEMORIZZATI NELLA PRIMA PARTE DELLA MEMORIA DI SUPPORTO.

C1) SE SI TROVANO UGUALI, ALLORA SI SMETTE DI CALCOLARE IL VALORE DI ALFA POICHE' TALE VALORE E' QUELLO SCRITTO NELLA SECONDA PARTE DELLA RIGA DI MEMORIA, E SI FA' SALIRE LA RIGA DI

MEMORIA CHE CONTIENE IL VALORE TROVATO FINO ALLA CIMA DELLA MEMORIA.

C2) SE NON SI TROVA, ALLORA APPENA SI E' CALCOLATO IL VALORE DI ALFA, FA SCENDERE DI UN LIVELLO TUTTI I VALORI MEMORIZZATI NELLA MEMORIA DI SUPPORTO, PERDENDO IL VALORE CONTENUTO SUL FONDO DELLA MEMORIA E SI MEMORIZZA NELLA RIGA IN CIMA ALLA MEMORIA (CHE E' STATA PRIMA SVUOTATA) LA TERNA DI VALORI { [V, PM], [ALFA] }.

D) SI PASSA IL VALORE DI ALFA AL CIRCUITO CHE PROCEDE AL CALCOLO DELL'INFERENZA E SI RITORNA AL PUNTO A).

Conclusioni

Si descrive in figura 1 uno schema funzionale a blocchi che implementa l'oggetto della nostra proposta di brevetto.

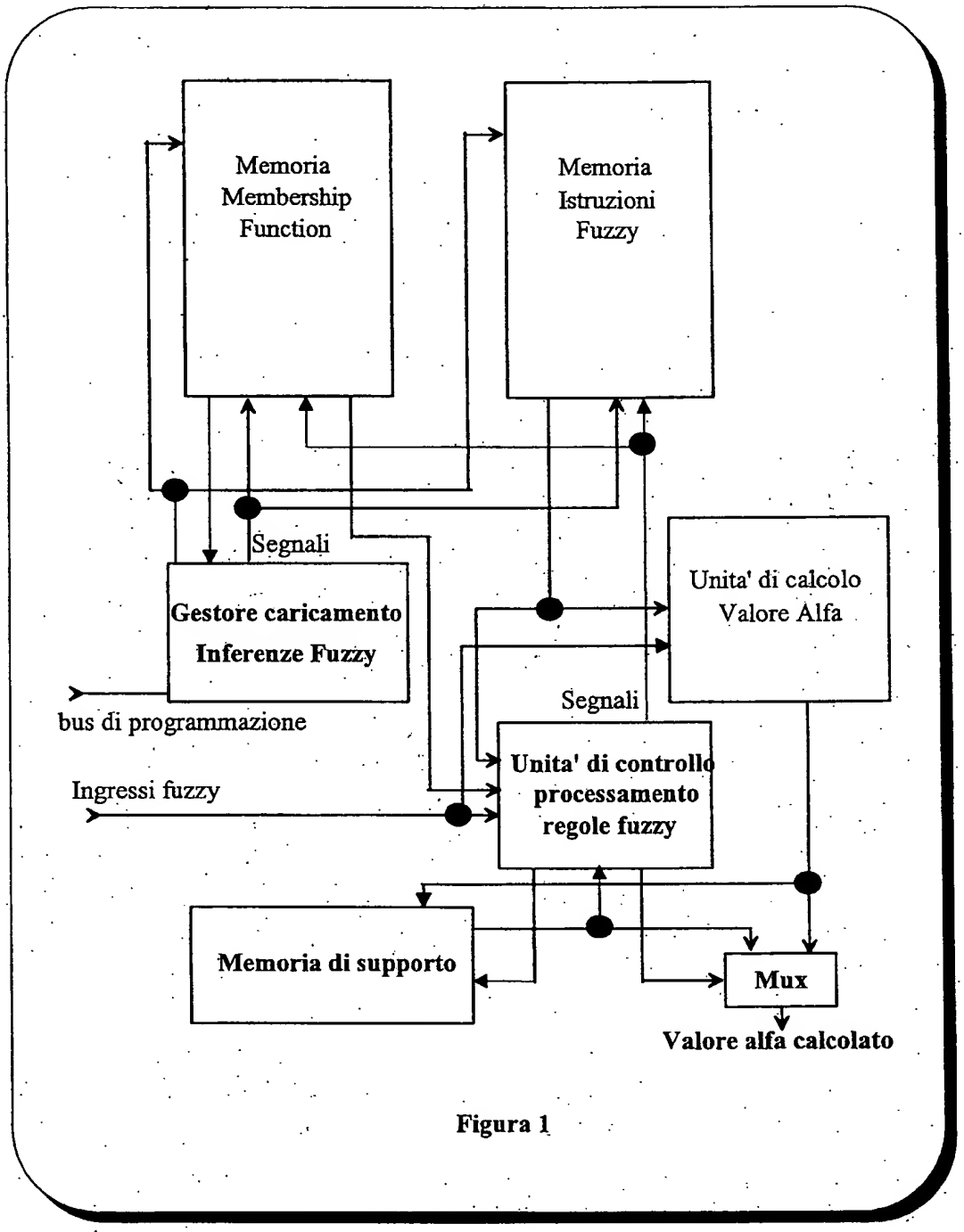

Memoria Membership Function
Memoria Istruzioni Fuzzy
Segnali
Gestore caricamento Inferenze Fuzzy
Unita' di calcolo Valore Alfa
bus di programmazione
Segnali
Unita' di controllo processamento regole fuzzy
Ingressi fuzzy
Memoria di supporto
Mux
Valore alfa calcolato

Figura 1

fig. 2

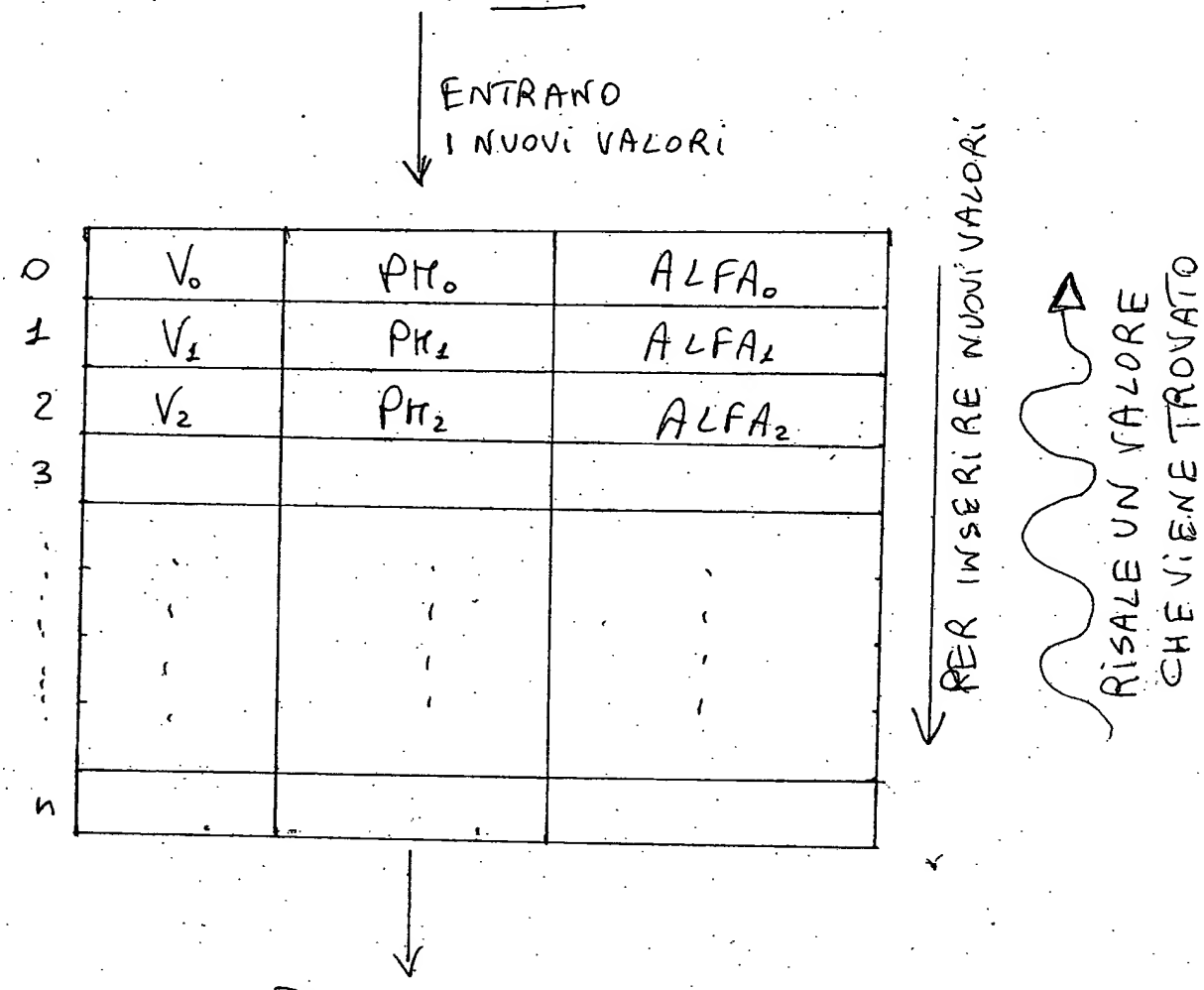


Figura 2

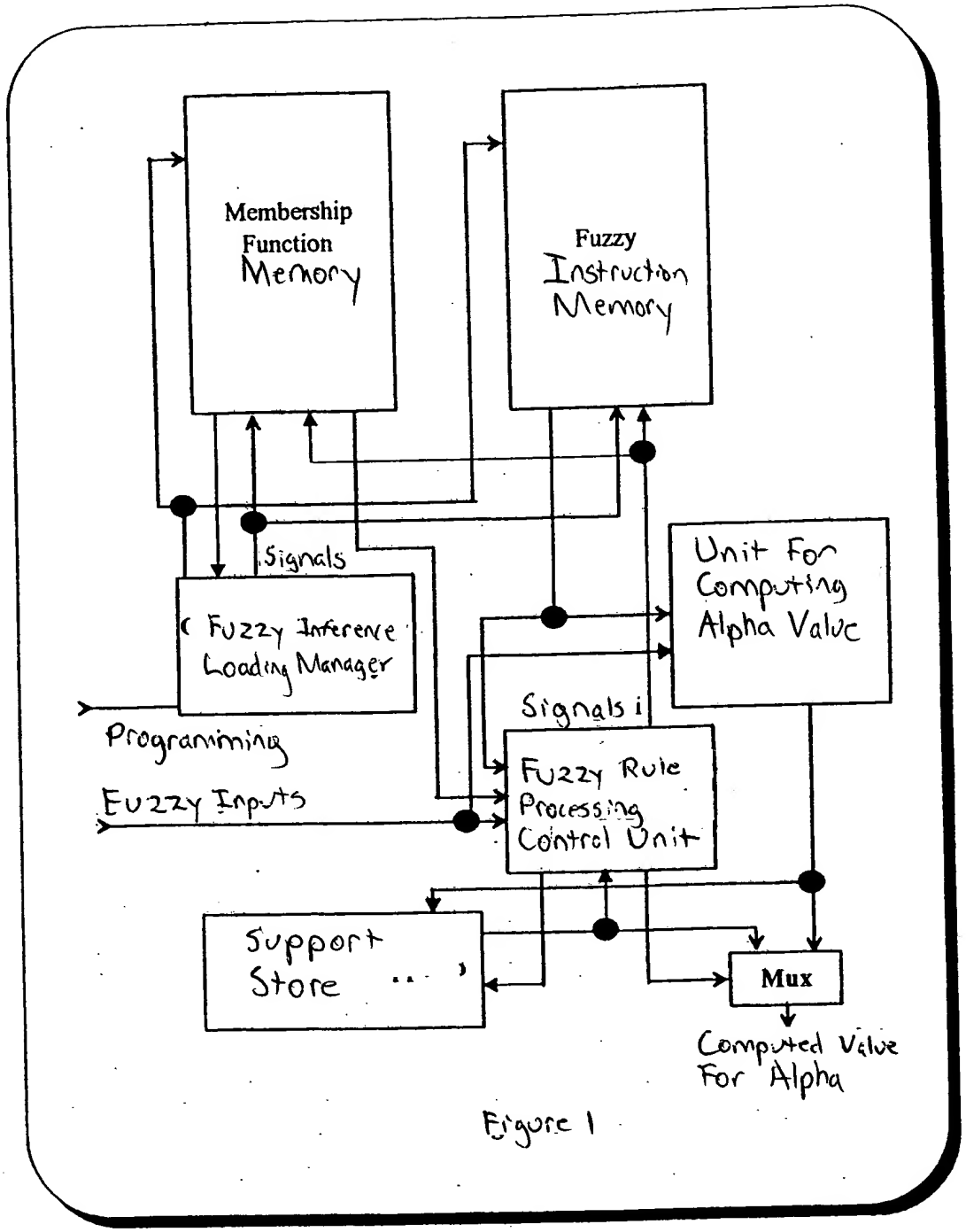
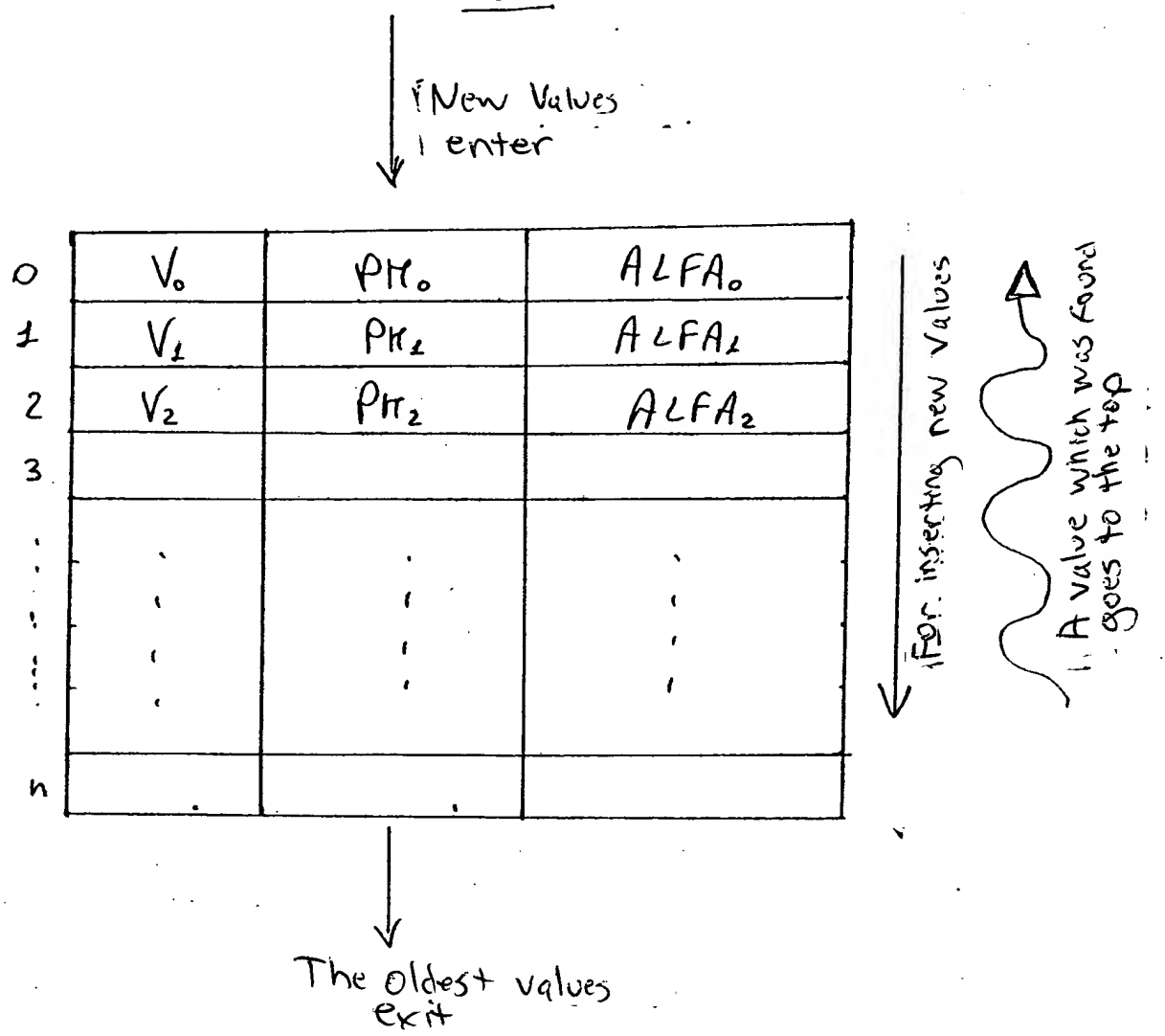

Membership Function Memory
Fuzzy Instruction Memory
Signals
Fuzzy Inference Loading Manager
Unit For Computing Alpha Value
Signals i
Programming
Fuzzy Inputs
Fuzzy Rule Processing Control Unit
Support Store
Mux
Computed Value For Alpha

Figure 1

fig. 2



Support Store

Figura 2